FIG. 1

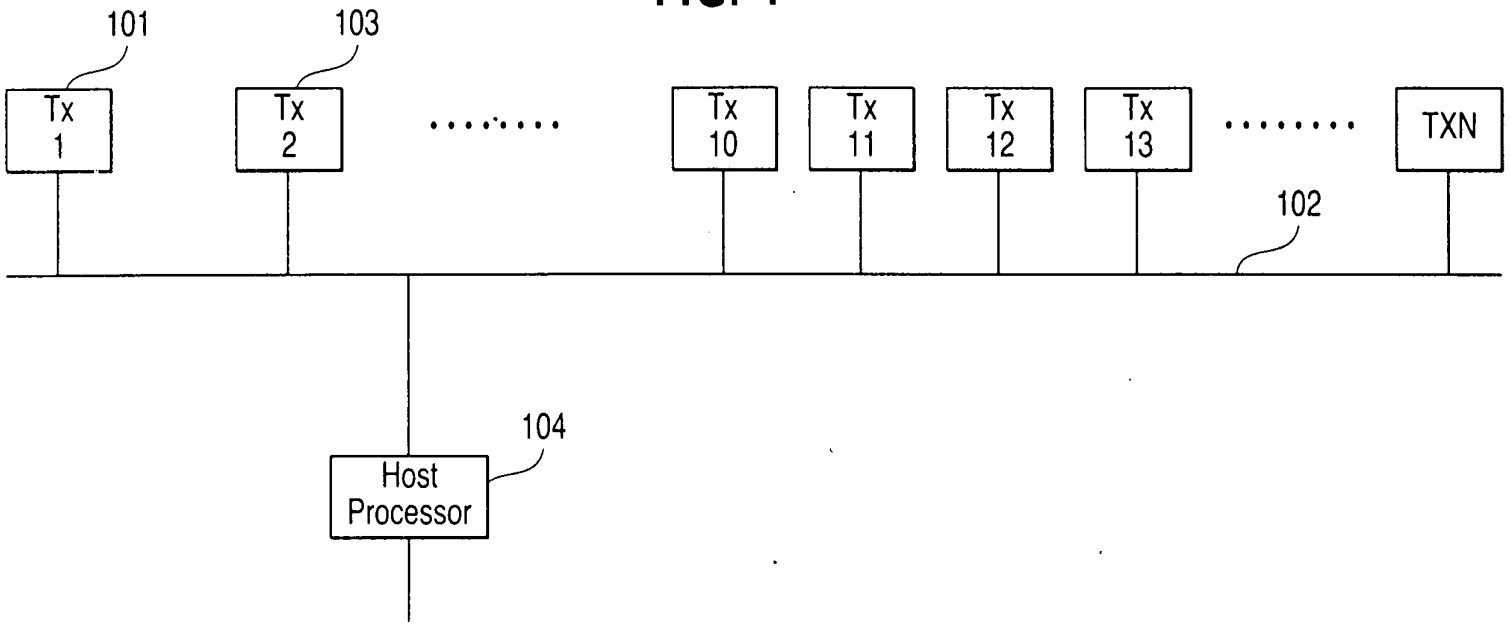

101
103
Tx 1
Tx 2
Tx 10
Tx 11
Tx 12
Tx 13
TXN
102
104
Host Processor

FIG. 2(a)

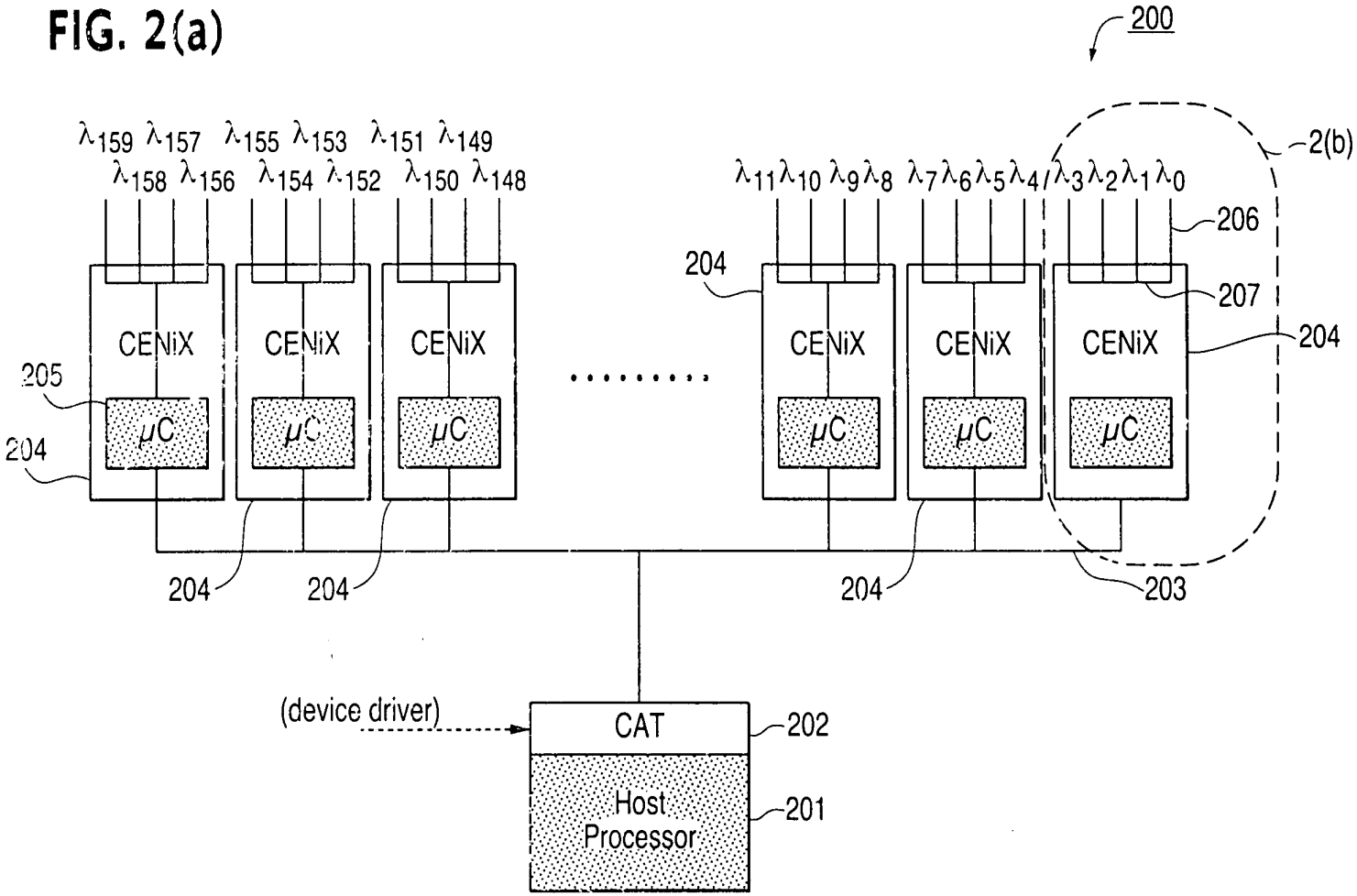

200
2(b)
λ159 λ157 λ155 λ153 λ151 λ149
λ158 λ156 λ154 λ152 λ150 λ148
λ11 λ10 λ9 λ8 λ7 λ6 λ5 λ4 λ3 λ2 λ1 λ0
206
207
204
CENiX
μC
205
204
204
204
204
203
(device driver)
CAT
202
Host Processor
201

FIG. 2(b)

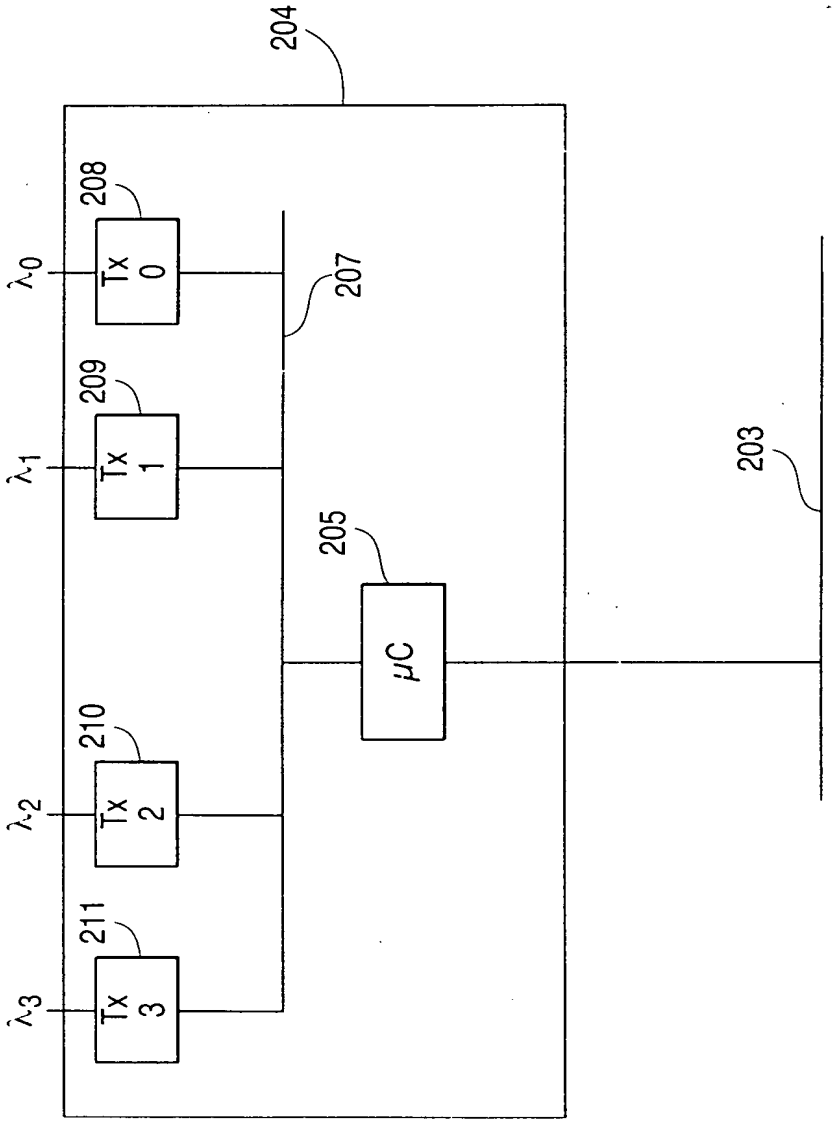


FIG. 2(c)

212

(Channel Access Table Example)

Channel Address	Physical Address	Memory Offset
0	0	0x000
1	0	0x200
2	0	0x400
3	0	0x600
4	4	0x000
5	4	0x200
6	4	0x400
7	4	0x600
⋮	⋮	⋮
156	156	0x000
157	156	0x200
158	156	0x400
159	156	0x600

FIG. 3

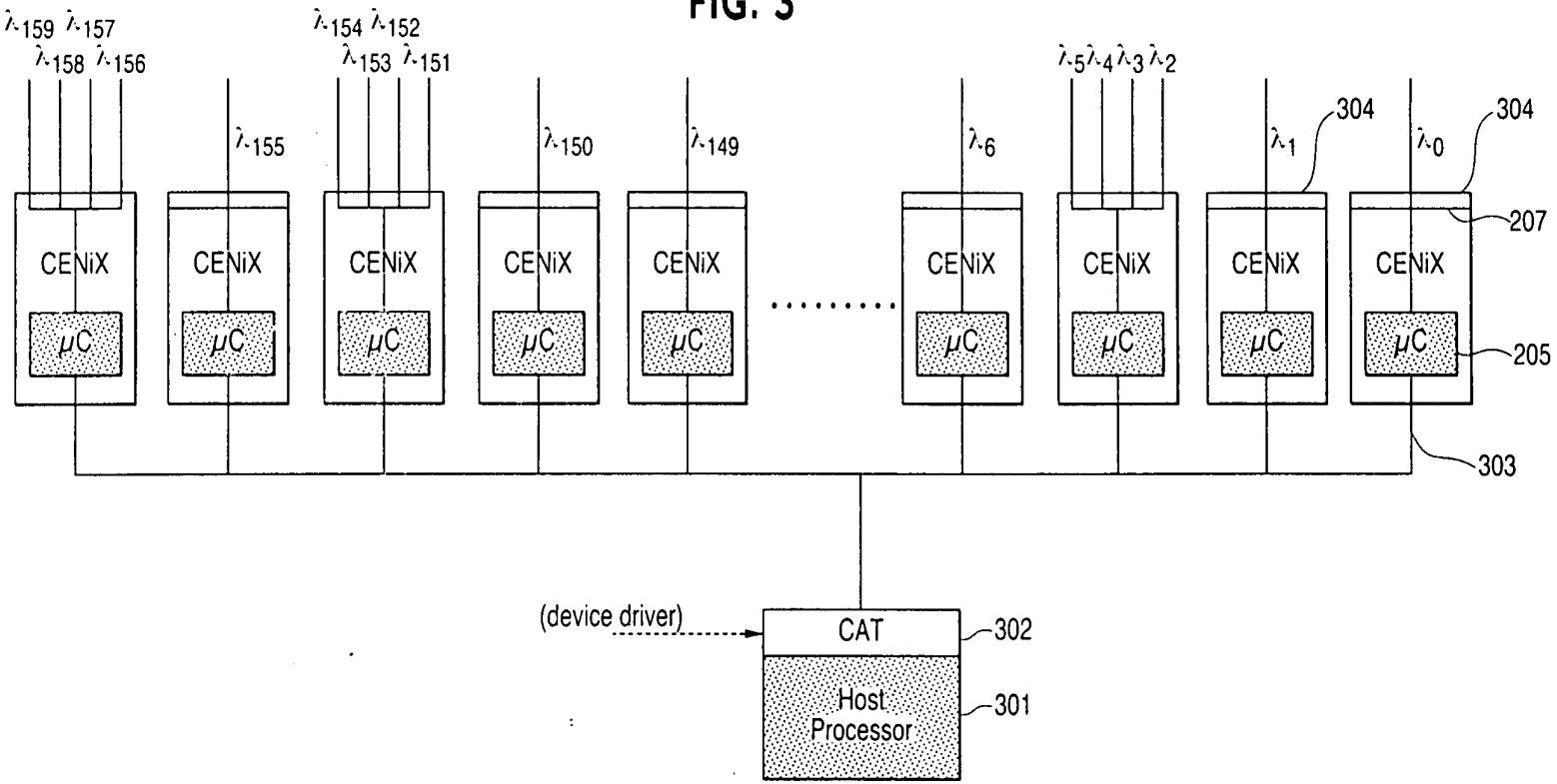

λ-159 λ-157
λ-158 λ-156
λ-155
λ-154 λ-152
λ-153 λ-151
λ-150
λ-149
λ-6
λ-5 λ-4 λ-3 λ-2
λ-1
λ-0
304
304
207
205
303
CENiX
μC
(device driver)
CAT
302
Host Processor
301

FIG. 4

400

(Channel Access Table Example)

Channel Address	Physical Address	Memory Offset
0	0	0x000
1	1	0x000
2	2	0x000
3	2	0x200
4	2	0x400
5	2	0x600
6	6	0x000
⋮	⋮	⋮
154	151	0x600
155	155	0x000
156	156	0x000
157	156	0x200
158	156	0x400
159	156	0x600

FIG. 5

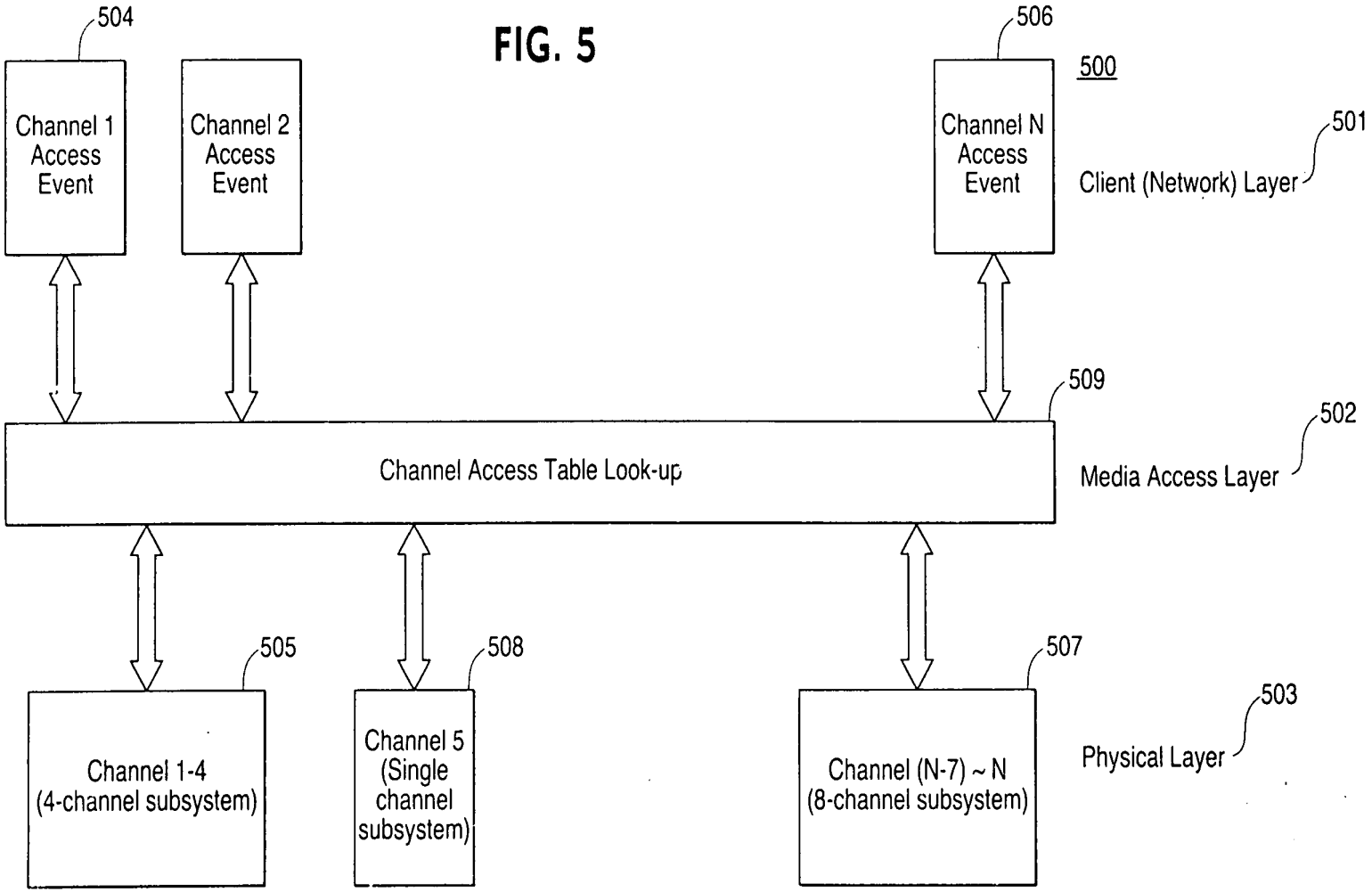
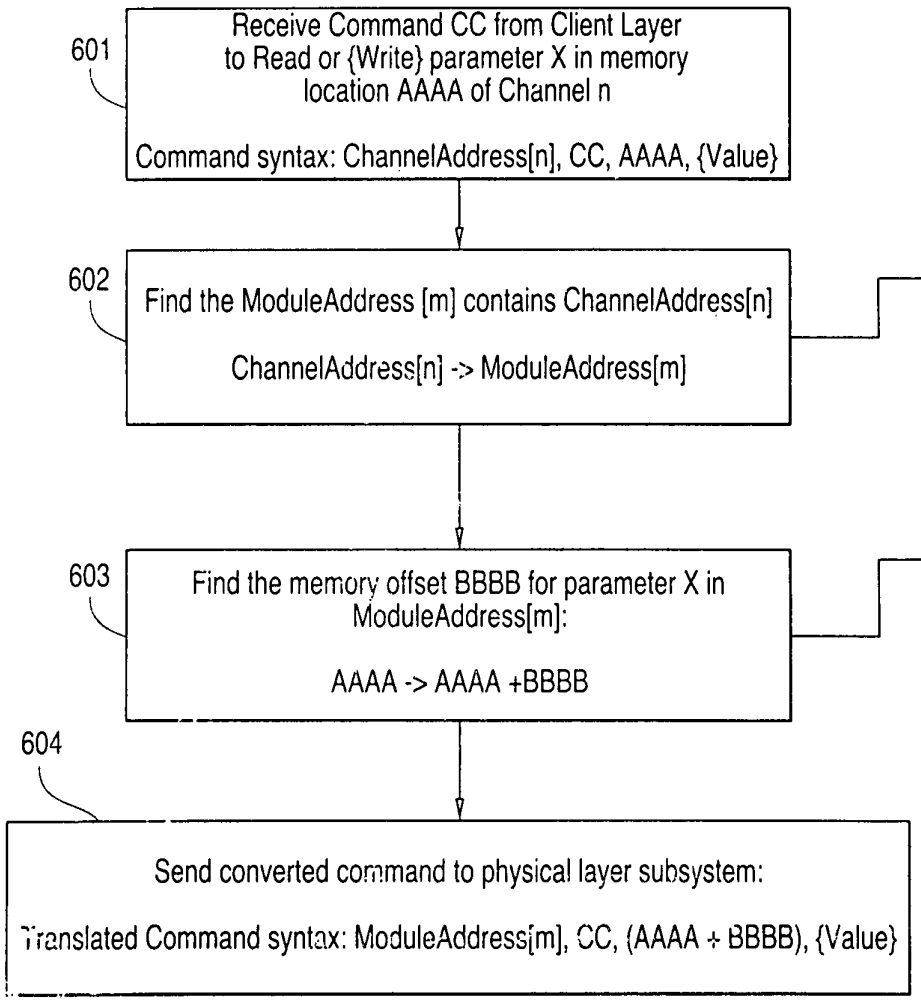

504
506
500
Channel 1 Access Event
Channel 2 Access Event
Channel N Access Event
501
Client (Network) Layer
509
502
Channel Access Table Look-up
Media Access Layer
505
508
507
503
Channel 1-4 (4-channel subsystem)
Channel 5 (Single channel subsystem)
Channel (N-7) ~ N (8-channel subsystem)
Physical Layer

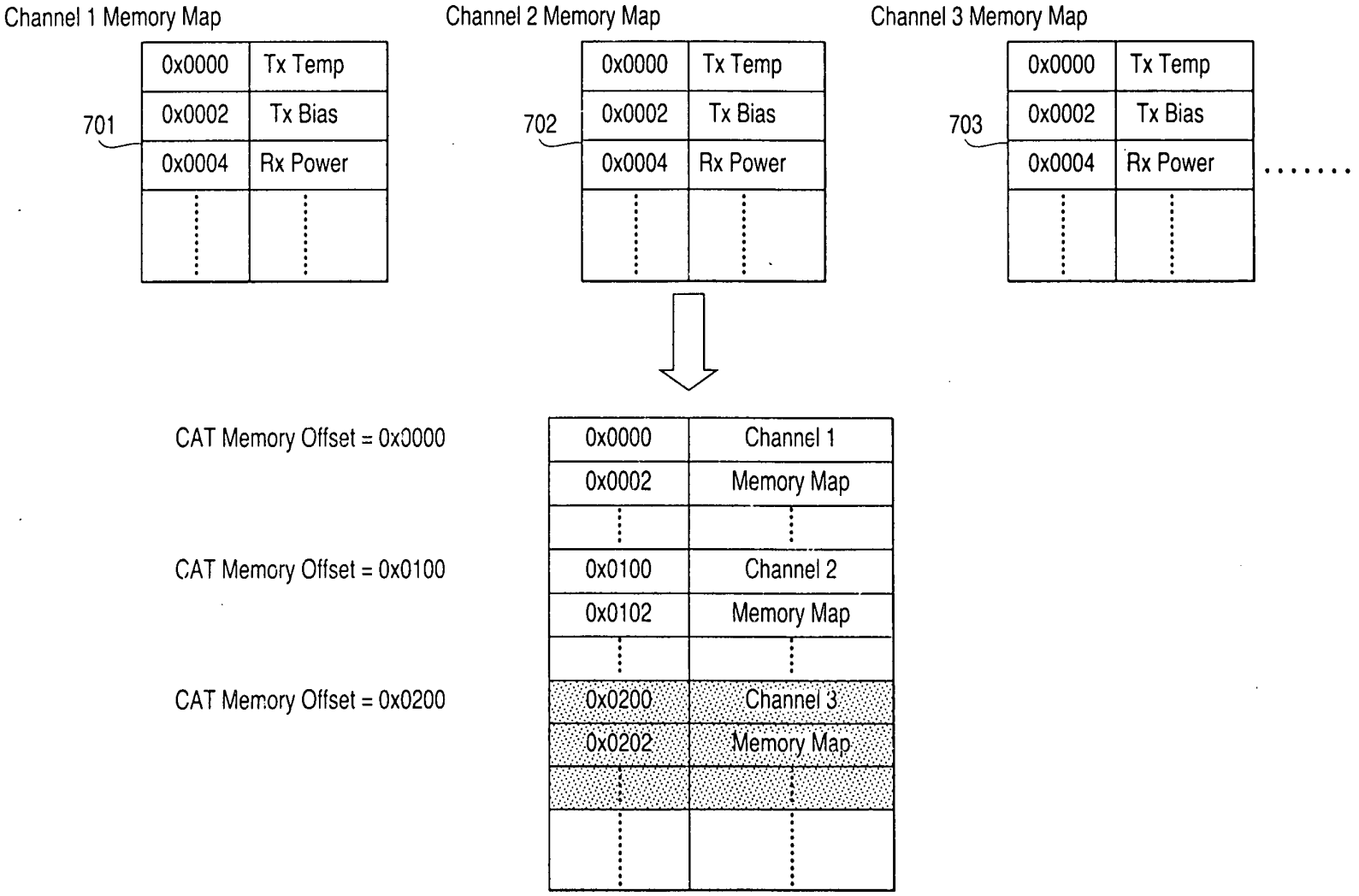
FIG. 6



(Channel Access Table Example)

Channel Address n	Module Address m	Memory Offset BBBB
0	0	0x000
1	1	0x000
2	2	0x000
3	2	0x200
4	2	0x400
5	2	0x600
6	6	0x000
⋮	⋮	⋮
154	151	0x600
155	155	0x000
156	156	0x000
157	156	0x200
158	156	0x400
159	156	0x600

FIG. 7


Channel 1 Memory Map
0x0000
Tx Temp
701
0x0002
Tx Bias
0x0004
Rx Power
Channel 2 Memory Map
0x0000
Tx Temp
702
0x0002
Tx Bias
0x0004
Rx Power
Channel 3 Memory Map
0x0000
Tx Temp
703
0x0002
Tx Bias
0x0004
Rx Power
CAT Memory Offset = 0x0000
CAT Memory Offset = 0x0100
CAT Memory Offset = 0x0200
0x0000
Channel 1
0x0002
Memory Map
0x0100
Channel 2
0x0102
Memory Map
0x0200
Channel 3
0x0202
Memory Map